In The United States Patent and Trademark Office

Appn Number:	10/718383
Appn. Filed:	11-19-03
Applicant:	T. Massingill
Appn. Title:	Semiconductor Package with Recess for Die
Examiner:	Alexander O. Williams

Mailed: March 18, 2006
At: Los Gatos, CA

Amendment C

Commissioner for Patents
PO Box 1450,
Alexandria, VA 22313-1450

Sir:

In response to the office action mailed Oct. 20, 2005, please amend the application as follows:

Specification:

Page 4 line 19 Modify paragraph 4 as follows.

"It is an object of the invention to provide a cavity down ball grid array package in which the recess has substrate circuitry" -- in the total recess area, and the circuitry allows multiple signal types and voltages under the die.

Page 5 line 11 Modify the last sentence of paragraph 3 as follows.

"Therefore, the recess has substrate circuitry" --, in the total recess area, -- "for electrical connections to the die, which are made by wirebonds, TAB, or solder balls."